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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	Hisashi YAMAUCHI
Serial No.:	10/736,934
Filed:	December 16, 2003
Title:	**METHOD OF GENERATING TEST PATTERN FOR INTEGRATED CIRCUIT**
Examiner:	
Group Art Unit:	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

S I R :

Prior to examination on the merits, please amend the subject application as follows:

IN THE CLAIMS

Please rewrite claims 1, 2, and 4 as follows: